Oct 10th – Ropar

Note Title 10-10-2011

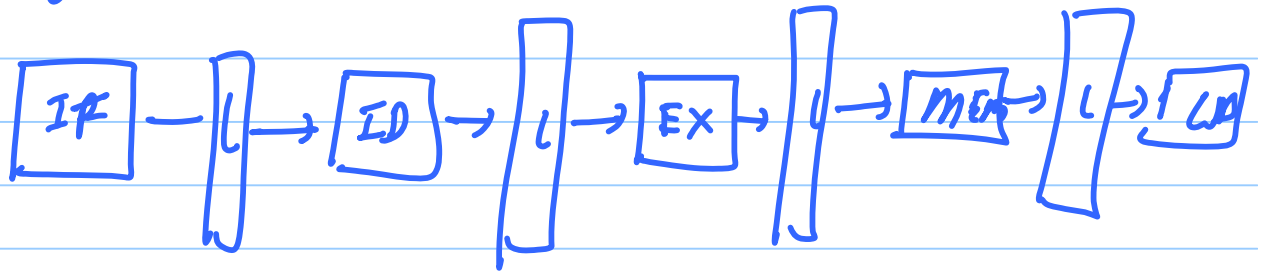
IF → Instruction Fetch

ID/RF → Instruction Decode / Reg. Read.

Ex → Execute

MEM → Memory

WB → Write back.



n instructions, k-stage pipeline.

Time: $1 \cdots k$

$2 \cdots k+1$

$\vdots$

$n \cdots n+k-1$

Time per Inst.: $\frac{n+k-1}{n} = 1 + \frac{k-1}{n}$

$k \ll n$

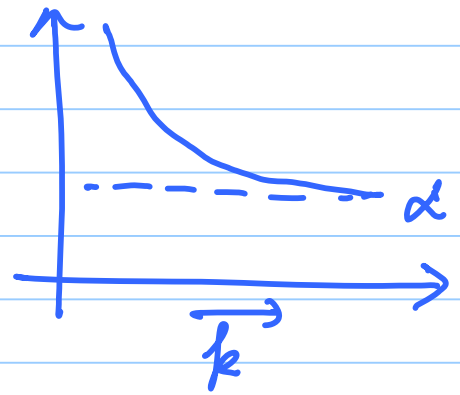
≈ 1

Total algorithmic work: W

k stages

algorithmic work/stage: $\frac{w}{k}$.

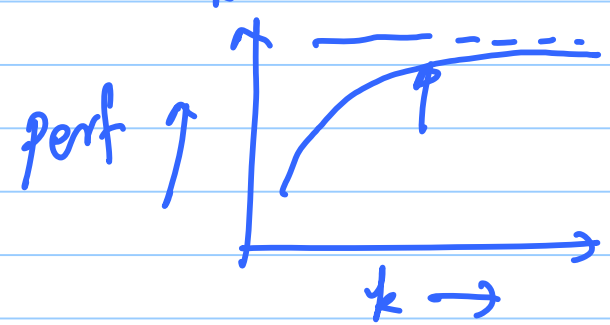
$t_{clk} = \frac{w}{k} + d$ ($d \rightarrow$ delay of the latch).



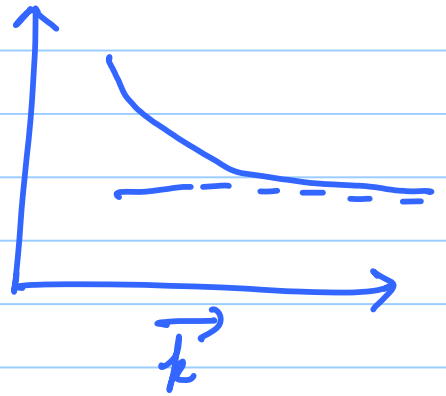
Perf $\propto$ IPC $\times f$

$t \propto$ CPI $\times t_{clk}$

$(\simeq 1)$ $(\frac{w}{k} + d)$



time



TODO:

1) Read chapter on pipelining + slides
2) Form groups of 3.
3) Buy a Java Book